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09/671,153	09/28/2000	Hiroyuki Fuse	016887/1013	8432

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EXAMINER	
THOMPSON, JAMES A	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/671,153	FUSE, HIROYUKI	
	Examiner	Art Unit	
	James A. Thompson	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005 and 23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 23 June 2005 have been fully considered but they are not persuasive.

Regarding page 7, line 19 to page 8, line 12: Without the software control signal (PS), no specific hidden pattern is added to the color image. Thus, Sasanuma (US Patent 5,719,681) does teach the limitations specifically recited in claim 1.

Regarding page 8, lines 13-30: The specific language of the claim states that "the specific hidden pattern is necessarily formed on an output image when *either* the hardware signal or the software signal exists" [emphasis added]. The claim language does not require that *only* the hardware signal or the software signal be present. If both the hardware signal and the software signal are present, as taught by Sasanuma, then the language of the claim is met.

2. Applicant's arguments filed 28 July 2005 have been fully considered but they are not persuasive.

While Examiner agrees with Applicant that the present amendments to the claims, filed 28 July 2005, do overcome the previously cited prior art (Sasanuma and Burns (US Patent 5,936,741)), additional art has been discovered which renders the claims obvious to one of ordinary skill in the art at the time of the invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasanuma (US Patent 5,719,681) in view of Peterson (US Patent 5,247,434).

Regarding claims 1 and 17: Sasanuma discloses an image forming apparatus (figure 2 of Sasanuma) for forming an image on an image forming medium (column 4, line 66 to column 5, line 3 of Sasanuma) and capable of forming a specific hidden pattern for specifying an apparatus (column 10, lines 30-33 of Sasanuma) at a specific position on said medium (column 10, lines 25-29 of Sasanuma), comprising a hardware control signal supplying unit (figure 2(409) of Sasanuma) for generating and supplying a hardware control signal (H) representing that data exists when color image data exists in the image forming apparatus (column 5, line 64 to column 6, line 6 of Sasanuma); a software control signal supplying unit (figure 2(414(portion)) of Sasanuma) for generating and supplying a software control signal (PS) for determining whether said specific hidden pattern is added to a color image (column 9, lines 55-60 of Sasanuma); and a specific hidden pattern control signal synthesizing circuit (figure 2(414(portion)) of Sasanuma) for synthesizing a control signal by which said specific hidden

pattern is necessarily formed on an output image when either the hardware signal or the software signal exists (column 10, lines 55-62 of Sasanuma). Said software control signal (PS) and said hardware control signal (H) are compared and the comparison result is used to determine if said specific hidden pattern is necessarily formed on an output image (column 10, lines 55-62 of Sasanuma). The signal generated by the comparison of said software control signal and said hardware control signal is said synthesized control signal. The CPU (figure 2(414) of Sasanuma) performs the operations of the software control signal supplying unit (column 9, lines 55-57 of Sasanuma) and the specific hidden pattern control signal synthesizing circuit (column 10, lines 55-57 of Sasanuma). The software control signal supplying unit and the specific hidden pattern control signal synthesizing circuit are portions of the software, physically embodied in electronic memory and executed by the CPU, that perform the functions of said software control signal supplying unit and said specific hidden pattern control signal synthesizing circuit.

Sasanuma does not disclose expressly that said specific hidden pattern is necessarily formed on said output image when either *one of* the hardware control signal or the software control signal exists and wherein the other one of the hardware control signal and the software control signal does not exist.

Peterson discloses, in a digital data processing system (figure 7 of Peterson), that an alarm is necessarily generated when either one of the hardware control signal or the software control signal exists and wherein the other of the hardware control signal and the software control signal

does not exist (column 21, lines 20-24 and lines 30-31 of Peterson). Since the hardware alarm signal is redundant to the software alarm signal (column 21, lines 20-24 and lines 30-31 of Peterson), then if the software alarm signal fails to trigger the alarm, the hardware alarm signal will trigger the alarm, and if the hardware alarm signal fails to trigger the alarm, the software alarm signal will trigger the alarm.

Sasanuma and Peterson are combinable because they are from similar problem solving areas, namely how to indicate states required for the initiation of a digital processing function through a combination of digital hardware and software signals. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use redundancy in the hardware and software signals so that, if one fails, the other will still be present to initiate the digital processing function, as taught by Peterson. The motivation for doing so would have been that, since either the hardware or the software signal can initiate the digital processing (such as an alarm) (column 21, lines 30-32 of Peterson), the digital processing system is more robust with regard to system errors. Therefore, it would have been obvious to combine Peterson with Sasanuma to obtain the invention as specified in claims 1 and 17.

Further regarding claim 1: The units and circuit of the apparatus of claim 17 provide the corresponding means of the apparatus recited in claim 1.

5. Claims 2-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasanuma (US Patent 5,719,681) in view of Peterson (US Patent 5,247,434) and Burns (US Patent 5,936,741).

Regarding claim 2: Sasanuma discloses image data supplying means (figure 2(210-1, 210-2, 210-3, and 401-406) of Sasanuma) for supplying color image data (column 5, lines 26-33 of Sasanuma). CCD line sensors (figure 2(210-1,210-2,210-3) of Sasanuma) detect RGB signals and output digital representation of the RGB signals (column 5, lines 26-33 of Sasanuma). Delay elements (figure 2(401-402) of Sasanuma) compensate for delays resulting from the physical spacing of said CCD line sensors (column 5, lines 34-37 of Sasanuma). The log converters (figure 2(403-405) of Sasanuma) convert brightness to density (column 5, lines 38-40 of Sasanuma) and the masking UCR circuit (figure 2(406) of Sasanuma) converts the RGB data to CMYK data (column 5, lines 40-46 of Sasanuma).

Sasanuma further discloses data existence/absence confirming means (figure 3(301-303,310) of Sasanuma) for confirming the existence/absence of image data in said image forming apparatus (column 5, lines 64-67 of Sasanuma). Portions (figure 3(301-303,301) of Sasanuma) of the determination circuit (figure 2(409) of Sasanuma) determine the existence/absence of specific originals that should not be copied (column 5, lines 64-67 of Sasanuma). The remaining portion is the maximum value circuit (figure 3(309) of Sasanuma), which outputs the determination signal, as discussed below.

Sasanuma further discloses that said hardware control signal supplying means generates and supplies said hardware

control signal (H) based on the existence/absence of image data confirmed by said confirming means (column 5, line 67 to column 6, line 3 of Sasanuma); that said software control signal supplying means generates and supplies said software control signal (PS) for adding said specific hidden pattern (column 9, lines 55-57 of Sasanuma); and that said control signal synthesizing means synthesizes said control signal in such a manner that said specific hidden pattern is necessarily formed on a color image (column 9, lines 54-60 of Sasanuma) when a usual image is formed on said image forming medium based on said hardware control signal (H) and said software control signal (PS) (column 10, lines 55-62 of Sasanuma).

Sasanuma further discloses hidden pattern generating means (figure 11(906-909) of Sasanuma) for generating said specific hidden pattern (column 9, lines 54-55 and column 9, line 65 to column 10, line 9 of Sasanuma). The registers (figure 11(906-909) of Sasanuma) store the hidden pattern values (column 9, lines 54-55 of Sasanuma). One of said patterns is specifically selected to be output (column 9, line 65 to column 10, line 4 of Sasanuma), and then added to the signal (column 10, lines 5-9 of Sasanuma).

Sasanuma further discloses pattern selecting means (figure 11(910) of Sasanuma) for selecting and outputting one of said specific hidden pattern based on said control signal synthesized by said control signal synthesizing means (column 9, line 65 to column 10, line 4 of Sasanuma); and image formation output signal synthesizing means (figure 11(912) of Sasanuma) which synthesizes said color image data supplied from said image data supplying means and said specific hidden pattern selected by said pattern

selecting means when said image data is inputted (column 9, lines 58-60 and column 10, lines 5-9 of Sasanuma).

Sasanuma in view of Peterson does not disclose expressly a test pattern generating means for generating and outputting a test pattern when a color image is not formed; that said pattern selecting means can further select said test pattern based on said control signal synthesized by said control signal synthesizing means; and that said image formation output signal synthesizing means outputs said test pattern selected by said pattern selecting means when said color image data is not inputted.

Burns discloses test pattern generating means (figure 2(28) of Burns) for generating and outputting a test pattern (figure 1(10) of Burns) when an image is not formed (column 8, lines 34-37 of Burns). The test pattern is printed on the entire medium, as clearly shown in figure 1(10) of Burns, therefore a particular scanned image is not being formed on said medium. Said test pattern can be selected based on a control signal (column 7, lines 55-60 of Burns).

Sasanuma in view of Peterson is combinable with Burns because they are from the same field of endeavor, namely digital image data control and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to including a test pattern generating means, as taught by Burns, and include the test pattern as a selection in the pattern selection means taught by Sasanuma. Said test pattern would then be output when there is no image data for said image forming apparatus, as taught by Burns, and output for each of the colors of the image forming apparatus. The motivation for

doing so would have been that a test pattern is used to properly calibrate the apparatus (column 7, lines 55-57 of Burns). Therefore, it would have been obvious to combine Burns with Sasanuma in view of Peterson to obtain the invention as specified in claim 2.

Regarding claim 3: Sasanuma discloses that said hardware control signal (H) generated by said hardware control signal supplying means is a signal which affects the addition of said specific hidden pattern (column 10, lines 58-62 of Sasanuma) and which avoids the normal formation of a usual image when said signal is abnormal (column 10, lines 62-65 of Sasanuma).

Regarding claim 4: Sasanuma discloses that said hardware control signal can be generated by software when said signal is set (figure 15 and column 10, lines 58-62 of Sasanuma). After said hardware control signal (H) is set, said software control signal (PS) is compared with said hardware control signal (column 10, lines 59-61 of Sasanuma). Since said comparison is performed with software (column 5, lines 55-58 and column 9, lines 55-57 of Sasanuma), it is inherent that, after said hardware control signal is set, said hardware control signal is generated by software. Otherwise, a comparison signal in software with which to compare said software control signal would not exist.

Regarding claim 5: Sasanuma discloses that said specific hidden pattern generated by said hidden pattern generating means is a special pattern formed by using colors or patterns which are hard to be identified by the naked eye (column 10, lines 10-14 of Sasanuma) in such a manner that a body of an image forming apparatus which has

formed an image can be specified from a reproduced image on said medium, even if a specific original which must not be inherently formed is formed on said medium (column 10, lines 14-19 of Sasanuma).

Regarding claim 6: Sasanuma discloses that said data existence/absence confirming means generates said hardware control signal for said hardware control signal supplying means (column 5, line 64 to column 6, line 3 of Sasanuma), when image data is supplied from said image data supplying means (column 5, lines 64-66 of Sasanuma).

Regarding claim 7: Sasanuma discloses that said control signal synthesizing means comprises circuitry for calculating a comparison of said hardware control signal supplied from said hardware control signal supplying means and said software control signal supplied from said software control signal supplying means (column 10, lines 55-62 of Sasanuma), and outputs a control signal by which a specific hidden pattern is selected and necessarily added to an image (column 10, lines 5-9 of Sasanuma). The CPU (figure 2(414) of Sasanuma) is inherently comprised of circuitry such as OR circuits, circuits that perform comparisons, AND circuits, and register circuits, among others. It is through applying software to a plurality of the circuits comprising CPUs that CPUs function. The functions that software codes perform determine which circuits comprising the CPU are used.

Sasanuma in view of Peterson does not disclose expressly that said OR circuit comprising said control signal synthesizing means calculates the logical OR of said hardware control signal supplied from said hardware control signal supplying means and said software control signal

supplied from said software control signal supplying means, and outputs a control signal by which a specific hidden pattern is necessarily added to an image when one of said hardware control signal and said software control signal is supplied.

Burns discloses specifically setting a test pattern to be printed by setting a control signal (column 8, lines 57-60 of Burns).

Sasanuma in view of Peterson is combinable with Burns because they are from the same field of endeavor, namely digital image data processing and control. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to specifically set said software control signal (PS) if a particular hidden pattern is desired. Therefore, if either said hardware control signal (H) or said software control signal (PS) is set to a particular hidden pattern, said hidden pattern will be selected for output. This effectively calculates a logical OR of said hardware control signal supplied from said hardware control signal supplying means and said software control signal supplied from said software control signal supplying means. The motivation for doing so would have been to select a set of image data that is appropriate to the current system conditions (column 8, line 66 to column 9, line 2 of Burns). Therefore, it would have been obvious to combine Burns with Sasanuma in view of Peterson to obtain the invention as specified in claim 7.

Regarding claim 8: Sasanuma discloses that said pattern selecting means comprises a selector (figure 11(910) of Sasanuma) for selecting said specific hidden pattern generated by said hidden pattern generating means

with said control signal (column 9, line 66 to column 10, line 4 of Sasanuma) for adding said specific hidden pattern to an output image as a selected input by said control signal synthesizing means (column 10, lines 5-9 of Sasanuma).

Regarding claim 9: Sasanuma discloses that said image formation output signal synthesizing means outputs to a printer engine (column 5, lines 4-7 of Sasanuma) an image formation signal by which a hidden pattern (column 10, lines 10-13 of Sasanuma) using a predetermined color or pattern is added (column 10, lines 29-33 of Sasanuma) at a predetermined position of an image to be formed (column 10, lines 27-29 of Sasanuma) by adding said specific hidden pattern supplied from said pattern selecting means to said image data supplied from said image data supplying means (column 10, lines 5-9 of Sasanuma).

Regarding claim 10: Sasanuma discloses that said image data supplying means comprises a yellow data supplying apparatus (figure 2(406) of Sasanuma) for supplying yellow image data to each of said image formation output signal synthesizing means and said hardware control signal supplying means (column 5, lines 41-46 of Sasanuma). The masking-UCR circuit (figure 2(406) of Sasanuma) supplies image data for each of the four CMYK colors (column 5, lines 41-46 of Sasanuma) including yellow image data (column 5, lines 43-44 of Sasanuma). The part of said masking-UCR circuit that specifically supplies the yellow image data corresponds to the yellow data supplying apparatus.

Regarding claim 11: Sasanuma discloses that said hardware control signal supplying means comprises a portion

which outputs a signal (H) (column 5, line 64 to column 6, line 3 of Sasanuma) selecting a specific hidden pattern (column 10, lines 55-62 of Sasanuma). Said hidden pattern is yellow image data (column 10, lines 10-11 of Sasanuma) formed in specific size blocks which are repeated throughout the output image (column 10, lines 27-29 of Sasanuma). Said yellow image data is output to an external printer (column 9, lines 61-64 of Sasanuma). The specific size blocks are therefore comprised of external yellow sub scanning direction (column 10, line 29 of Sasanuma) image data based on said yellow image data (column 10, lines 10-11 of Sasanuma). The output of said hardware control signal supplying means would therefore be a -YVDEN signal enabling an external yellow sub scanning direction image based on said yellow image data.

Regarding claim 12: Sasanuma discloses that said control signal synthesizing means comprises circuitry for calculating a comparison of said -YVDEN signal (H) supplied from said hardware control signal supplying means and an output signal (PS) from a specific pattern addition signal generating register (column 10, lines 55-62 of Sasanuma), and outputs a control signal by which a specific hidden pattern is selected and necessarily added to an image (column 10, lines 5-9 of Sasanuma). The CPU (figure 2(414) of Sasanuma) is inherently comprised of circuitry such as OR circuits, circuits that perform comparisons, NOT circuits, and register circuits, among others. It is through applying software to a plurality of the circuits comprising CPUs that CPUs function. The functions that software codes perform determine which circuits comprising the CPU are used. The use of said circuits would therefore

further include a register which generates a signal (PS) for adding a specific pattern since said signal requires storage in some form. Furthermore, it would be an obvious design choice to use a single active-low signal bit for said -YVDEN signal (H) and a single active-high signal bit for said output signal (PS) from said specific pattern addition signal generating register, since use of such single bit signals would simply indicate whether or not a hidden pattern is to be used. The use of a single bit for a signal and the use of an active low signal are old, well-known and commonly used in the digital data processing arts.

Sasanuma in view of Peterson does not disclose expressly that said control signal synthesizing means comprises a NOT circuit which inverts said external yellow sub scanning direction image enabled signal (-YVDEN) outputted from said -YVDEN output portion as said hardware control signal supplying means and an OR circuit for calculating the logical OR of an output from said NOT circuit and an output signal from a specific pattern addition signal generating register as said hardware control signal supplying means.

Burns discloses specifically setting a test pattern to be printed by setting a control signal (column 8, lines 57-60 of Burns).

Sasanuma in view of Peterson is combinable with Burns because they are from the same field of endeavor, namely digital image data processing and control. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to specifically set said output signal (PS) if a particular hidden pattern is desired.

Therefore, if either said -YVDEN signal (H) or said output signal (PS) is set for outputting a hidden pattern, then a hidden pattern will be selected for output. Said -YVDEN signal (H) would have to be inverted in order to coincide with the same digital logic as said output signal (PS). This effectively calculates a logical OR of the inverted -YVDEN signal and said output signal. The motivation for doing so would have been to select image data when said image data is appropriate to the current system conditions (column 8, line 66 to column 9, line 2 of Burns). Therefore, it would have been obvious to combine Burns with Sasanuma in view of Peterson to obtain the invention as specified in claim 12.

Regarding claim 13: Sasanuma discloses that said data existence/absence confirming means generates a hardware control signal in said hardware control signal supplying means (column 5, line 64 to column 6, line 3 of Sasanuma). Said hardware control signal (H) selects a specific hidden pattern (column 10, lines 55-62 of Sasanuma). Said specific hidden pattern is comprised of specific size blocks of image data which are tiled across the output image (column 10, lines 27-29 of Sasanuma) and printed on an external printer (column 9, lines 61-64 of Sasanuma). An external printer inherently requires some form of control signal for controlling drive of a paper carrying motor for carrying paper. Said paper is the image forming medium (column 5, lines 16-19 of Sasanuma). Therefore, the hardware control signal is based on a control signal for controlling drive of a paper carrying motor for carrying paper as said image forming medium.

Regarding claim 14: Sasanuma discloses that said pattern selecting means comprises a selector (figure 11(910) of Sasanuma) for selecting said specific hidden pattern generated by said hidden pattern generating means with said control signal (column 9, line 66 to column 10, line 4 of Sasanuma) by which said specific hidden pattern is added to an output image by said control signal synthesizing means as a selected input (column 10, lines 5-9 of Sasanuma).

Regarding claim 15: Sasanuma discloses that said hidden pattern generating means comprises a specific pattern generating portion (figure 11(909-910) of Sasanuma) for generating a specific hidden pattern (column 9, lines 54-55 and column 9, line 65 to column 10, line 4 of Sasanuma). A specific pattern (P4) is stored in a register (figure 11(909) of Sasanuma) (column 9, lines 54-55 of Sasanuma) and selected by a selector (figure 11(910) of Sasanuma) when the appropriate input signal is received (column 9, line 65 to column 10, line 4 of Sasanuma).

Regarding claim 16: Sasanuma discloses that said image formation output signal synthesizing means comprises an adder (figure 11(912) of Sasanuma) which outputs to a printer engine an image formation signal (column 10, lines 5-9 of Sasanuma) by which a hidden pattern using a predetermined color or pattern is added (column 10, lines 10-11 of Sasanuma) at a predetermined position of an image to be formed (column 10, lines 27-29 of Sasanuma) by adding said image data supplied from said image data supplying means and said specific hidden pattern supplied from said pattern selecting means (column 10, lines 5-9 of Sasanuma).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A. Thompson whose telephone number is 571-272-7441. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James A. Thompson
Examiner
Art Unit 2624

JAT
08 August 2005

THOMAS D. LEE
PRIMARY EXAMINER